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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,849	03/15/2005	Xuanming Shi	05504-PCT	1881

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EXAMINER	
WOOLCOCK, LENWORTH A	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
03/27/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/527,849	SHI, XUANMING	
	Examiner	Art Unit	
	LENWORTH WOOLCOCK	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-11,16,19-21,23-25 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-6,9-11,16,19-21,23-25 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/13/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the Amendment filed 03/15/2005, in relation to Application Number: 10/527849. Claims 7, 8, 12-15, 17, 18, 22, 26, 27, 29, and 30 have been cancelled. Claims 5, 6, 9, 16, 19, and 20 have been amended. No new claims have been added. Therefore, claims 1-6, 9-11, 16, 19-21, 23-25, and 28 are currently pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 9, 16, 19, 20, 23, 25, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al (US 5506375) in view of Yamanami et al (US 4878553).

Consider claim 1, Kikuchi discloses an electronic whiteboard with a built-in electromagnetic induction layer of wire lattice **(see col 1 lines 8-13)** comprising: a writing input portion **(see fig 2,(24))**, a covering frame portion formed around the periphery of the writing input portion **(see fig 2, (11))**, and a control circuit **(see fig 2, (22))**, wherein the writing input portion has multiple layers **(see fig 2, (13) (14)(15) and (16))** and is enclosed in the frame **(see fig 2)**, the writing input portion includes a surface writing layer **(see fig 2, (24))**, an underlayer **(see fig 2, (16))**, an input induction

layer which is formed between the surface writing layer and the underlayer **(see col 5 lines 21-27)**, and the wires are insulated with each other at the crossing points **(see col 4 lines 19-20)**. Kikuchi does not specifically disclose the input induction layer connected to the control circuit, characterized in that the induction layer is a wire lattice winded and interlaced separately by wires along the X and Y axes, and space formed within each lattice unit constitutes one induction cell. Yamanami discloses a input induction layer connected to the control circuit by its output **(see fig 1)**, characterized in that the induction layer is a wire lattice winded and interlaced separately by wires along the X and Y axes **(see col 10 lines 40-46)** and an space formed within each lattice unit constitutes one induction cell **(see col 4 lines 64-67, space formed by loop coils indicate induction cell).**

It would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Kikuchi, and have the input induction layer connected to the control circuit, characterized in that the induction layer is a wire lattice winded and interlaced separately by wires along the X and Y axes, and space formed within each lattice unit constitutes one induction cell, as taught by Yamanami, thus attaining a high degree of precision, as discussed by Yamanami **(see col 1 lines 60-66)**.

Consider claim 2, Kikuchi discloses the area of said induction layer is the same as or smaller than those of the writing layer and the underlayer **(see fig 2, (20) and (21) are smaller in size than the writing layer).**

Consider claim 3, Kikuchi discloses the induction layer, which is smaller than the area of the writing layer and the underlayer **(see fig 2, (20) and (21) is smaller than**

(11) and (12)), is positioned at one side or in the center of the writing scope of the writing input portion **(see fig 2, (20) and (21) are centered)**.

Consider claim 4, Kikuchi discloses a shielding layer is provided behind the induction layer in order to enhance the anti-interference ability of the device **(see fig 2, (16))**.

Consider claim 5, Kikuchi discloses a buffering layer is provided between the induction layer and the underlayer, or between the induction layer and the shielding layer **(see fig 2, (15))**.

Consider claim 6, Kikuchi discloses the wires are entirely covered or coated by an insulating layer on the surface, such as the wires are enameled wires **(see col 4 lines 19-20)**.

Consider claim 9, Kikuchi discloses more than one induction layer are overlaid together and the induction cells on each induction layer are interlaced one another, and the induction cells on each induction layer are at the same or different intervals **(see fig 2, (20) and (21))**.

Consider claim 16, Kikuchi does not specifically disclose control circuit includes circuits for signal amplification, filtering acquisition and data processing, and is provided with signal output control circuit and/or storing device; said signal output device comprises electrical cable with standard computer data interface or wireless data switching means; said signal output device connects with a computer and/or a printer, or an external data storing device, or connects with a telephone line by an auxiliary modem. Yamanami discloses control circuit includes circuits for signal amplification

(see fig 2, (51)), filtering acquisition **(see fig 2, (54) and (55))** and data processing **(see fig 2, (70))**, and is provided with signal output control circuit and/or storing device **(see col 8 lines 62-67)**; said signal output device connects with a computer and/or a printer, or an external data storinq device, or connects with a telephone line by an auxiliary modem **(see col 9 lines 20-25)**.

It would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Kikuchi, and have control circuit includes circuits for signal amplification, filtering acquisition and data processing, and is provided with signal output control circuit and/or storing device; said signal output device comprises electrical cable with standard computer data interface or wireless data switching means; said signal output device connects with a computer and/or a printer, or an external data storinq device, or connects with a telephone line by an auxiliary modem, as taught by Yamanami, thus providing a means for supplying and receiving appropriate signals to and from the electromagnetic induction layer.

The combination of Kikuchi and Yamanami does not specifically disclose said signal output device comprises electrical cable with standard computer data interface or wireless data switching means, i.e. radio frequency transceiver. It would have been obvious to one skilled in the art at the time the invention was made to have the signal output device comprise electrical cable with standard computer data interface or wireless data switching means, thus supplying method of transferring data to and from the connected computer.

Consider claim 19, Kikuchi discloses the control circuit is formed in the body of the electronic whiteboard **(see fig 1a)**. Kikuchi does not specifically disclose the control circuit and the induction layer are directly connected in a whole, and components of the control circuit are positioned on the output end of the wire lattice. Yamanami discloses the control circuit and the induction layer are directly connected in a whole **(see fig 1, control circuit is directly connected to induction layer by (23) and (24))**, and components of the control circuit are positioned on the output end of the wire lattice **(see col 6 lines 58-62)**.

Consider claim 20, the combination of Kikuchi and Yamanami discloses the components of the control circuit are provided on a printed wiring board, and the output end of the wire lattice of the induction layer is connected to the corresponding input terminal on the printed circuit board **(see above)**. The combination of Kikuchi and Yamanami does not specifically disclose the printed wiring board being separated from the induction layer, and the output end of the wire lattice of the induction layer is connected to the corresponding input terminal on the printed circuit board by means of pressure-connection, plug-in connection or welding connection. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the printed wiring board being separated from the induction layer, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. *Nerwin v. Erlicnrnan,* 168 USPQ 177, 179. It would have been an obvious matter of design choice to have the output end of the wire lattice of the induction layer is connected to the corresponding

input terminal on the printed circuit board by means of pressure-connection, plug-in connection or welding connection, since applicant has not disclosed that means of pressure-connection, plug-in connection or welding connection solves any stated problem or is for any particular purpose.

Consider claim 23, the combination of Kikuchi and Yamanami does not specifically disclose the control circuit is installed outside the body, and connected to the body through the electrical connection means, the output of the wire lattice of the induction layer is connected with the output interface of the induction layer by means of pressure-connection, plug-in connection or welding-connection, and an interface matching the electrical connection means of the induction layer is provided on the control circuit. It would be obvious to one having ordinary skill in the art at the time of invention to place the control circuit outside the body for the commonly understood benefits of improving interchangeability through separate manufacturing of parts and preventing erroneous waste during the manufacturing process, both common goals within the art. It would be obvious to connect these elements through an electrical means for the unit to appropriately function. It would be an obvious to one having ordinary skill in the art to use any of these connections as they are well known and commonly used in the art, and use of one over the other is a mere matter of manufacturing cost determinations and design structure. It would be obvious to one having ordinary skill in the art at the time of invention to match interfaces in order to ensure the commonly understood benefits of compatibility of elements for proper functioning of the device, a common goal within the art.

Consider claim 25, the combination of Kikuchi and Yamanami does not specifically disclose the output interface of the induction layer and the interface of the control circuit is a pin-type connection means, or a flexible printed wiring means, or a PIN-PIN connection means, or a welding spot (VGA) thermal-melted connection means, or an ultrasonic welding device, or a solder-plate welding device, or a puncturing connection means. However, it would be an obvious to one having ordinary skill in the art to use any of these connections as they are well known and commonly used in the art, and use of one over the other is a mere matter of manufacturing cost determinations and design structure.

Consider claim 28, the combination of Kikuchi and Yamanami does not specifically disclose the writing input portion and the covering frame around the writing input portion is made of flexible and windable material, and the body of the electronic whiteboard is windable and portable. However, it would be an obvious to one having ordinary skill in the art to use flexible, windable and portable material to ensure durability and ease of use.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al (US 5506375) in view of Yamanami et al (US 4878553) in further view of Yamanami et al (US 2002/0044208) here in after referred to as "Yam".

Consider claim 10, the combination of Kikuchi and Yamanami discloses a electronic whiteboard with a built-in electromagnetic induction layer of a wire lattice. The combination of Kikuchi and Yamanami does not specifically disclose the wire lattice

is attached and fixed on an insulating membrane by thermal pressing and thermal melting, so as to form a wire electromagnetic induction layer with the insulating membrane. Yam discloses the wire lattice is attached and fixed on an insulating membrane by thermal pressing and thermal melting, so as to form a wire electromagnetic induction layer with the insulating membrane **(see par [0360]-[0361], where Yam discloses method of attaching wire lattice to an insulating membrane)**.

It would have been obvious to one skilled in the art at the time the invention was made to modify the invention of the combination of Kikuchi and Yamanami, and have the wire lattice is attached and fixed on an insulating membrane by thermal pressing and thermal melting, so as to form a wire electromagnetic induction layer with the insulating membrane, as taught by Yam, thus creating a better-quality attachment between the surfaces.

Consider claim 11, the combination of Kikuchi and Yamanami does not specifically disclose the insulating membrane is made of film material. Yam discloses the insulating membrane is made of film material **(see par [0360]-[0361])**.

Claims 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al (US 5506375) in view of Yamanami et al (US 4878553) in further view of Keely et al (US 2002/0063694).

Consider claims 21 and 24, the combination of Kikuchi and Yamanami does not specifically disclose the output end of the wire lattice of the induction layer is formed

between a hard pressing strip and the printed circuit board; a buffering layer is provided between the hard pressing strip and the output end of the wire lattice; and the hard pressing strip, the buffering layer and the output end of the wire lattice are overlaid on the printed circuit board by means of the screwing-conjunction; the output end of the wire lattice is connected to the corresponding input terminal on the printed circuit board. Keely discloses the output end of the wire lattice of the induction layer is formed between a hard pressing strip and the printed circuit board **(see fig 1, (36), and par [0032]-[0037])**; a buffering layer is provided between the hard pressing strip and the output end of the wire lattice **(see fig 1, (50), and par [0032]-[0037])**; the output end of the wire lattice is connected to the corresponding input terminal on the printed circuit board **(see fig 1, (72) and par [0032]-0042])**.

It would have been obvious to one skilled in the art at the time the invention was made to modify the invention of the combination of Kikuchi and Yamanami, and have the output end of the wire lattice of the induction layer formed between a hard pressing strip and the printed circuit board; a buffering layer provided between the hard pressing strip and the output end of the wire lattice; the output end of the wire lattice connected to the corresponding input terminal on the printed circuit board, as taught by Keely, thus preventing unwanted adsorption of magnetic fields, as discussed by Keely **(see par [0035])**.

Keely discloses bonding the layers together **(see par [0035])**. Keely does not specifically disclose the hard pressing strip, the buffering layer and the output end of the wire lattice are overlaid on the printed circuit board by means of the screwing-

conjunction. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use means of the screwing-conjunstion, since it has been commonly understood as having benefits of a stronger bond between the layers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LENWORTH WOOLCOCK whose telephone number is (571)270-5152. The examiner can normally be reached on M-F 8:30am - 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lenworth Woolcock/
Examiner, Art Unit 2629

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629